

Introduction to FPGAs Hardware

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Programming Models and OS for FPGA-based Architectures team

Outline

- FPGAs from 10000 feet...
- ... and coming down
- FPGA components
- Generating FPGA configurations

FPGAs: 10000 feet view

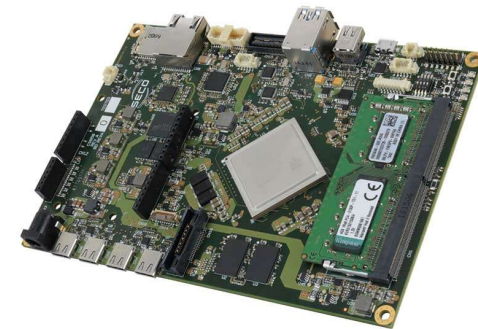
- The boards

Discrete (to be connected to PCIe)



source: docs.xilinx.com

Integrated (standalone)



source: www.axiom-project.eu

FPGAs: 10000 feet view

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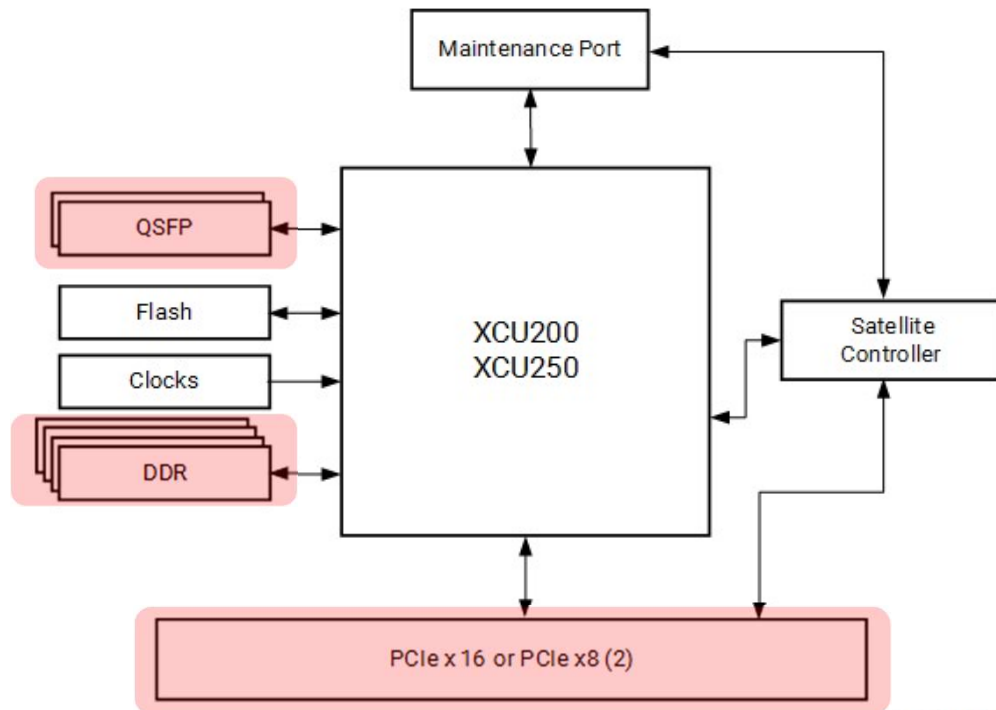
source: www.axiom-project.eu

AMD-Xilinx
Versal
Alveo
VCU128
...
Intel-Altera
Agilex
Stratix
Arria
...

AMD-Xilinx
Zynq 7000
Zynq Ultrascale+
...
Intel-Altera
Cyclone
Max
...

FPGAs: 5000 feet view

- Alveo U200 card basic hardware blocks



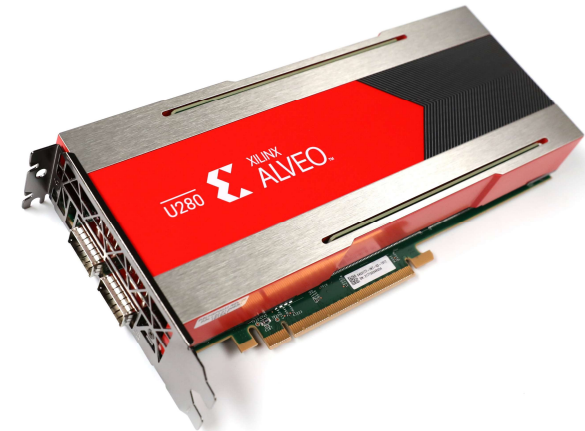
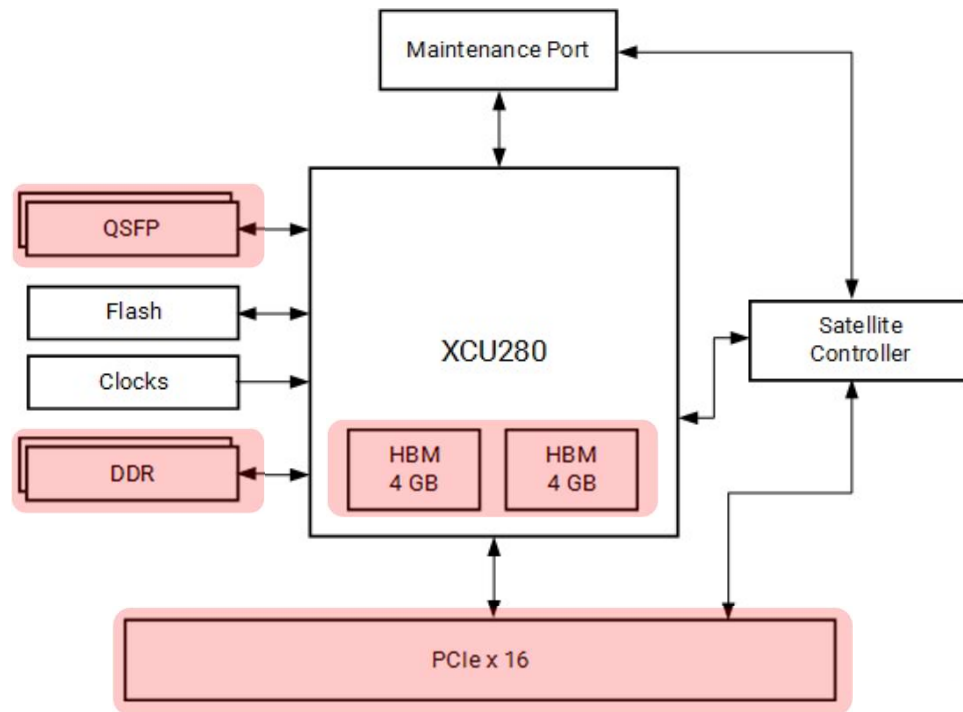
X23520-111319

source: docs.xilinx.com



FPGAs: 5000 feet view

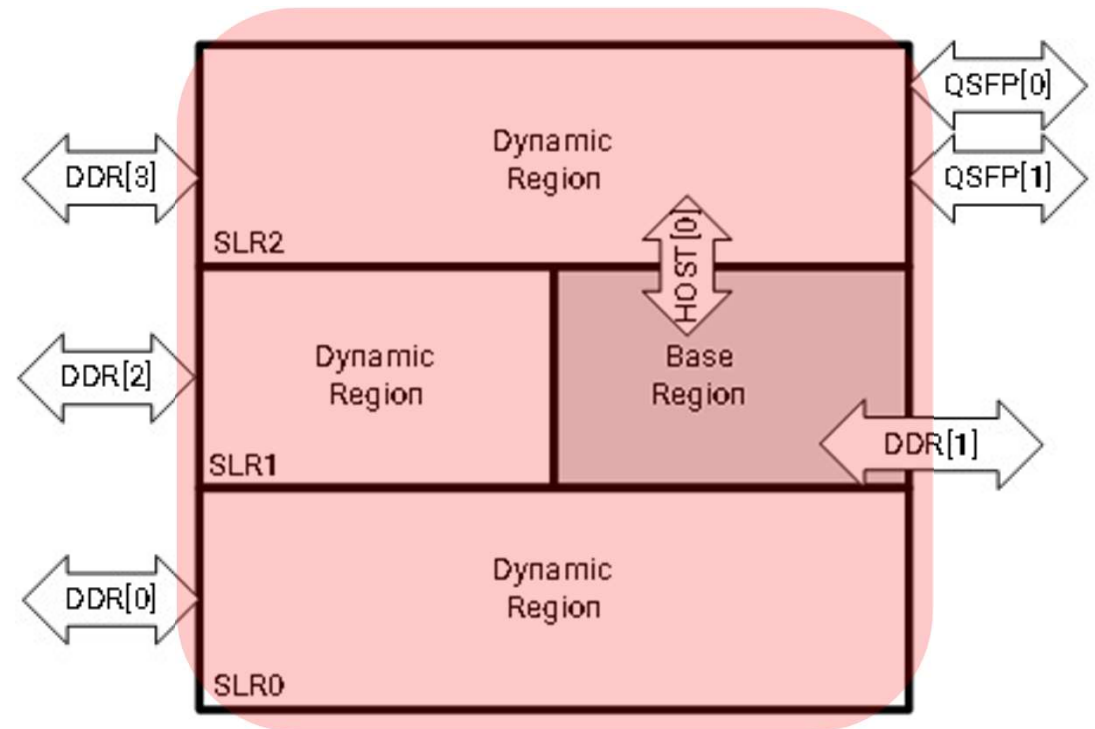
- Alveo U280 card basic hardware blocks



source: docs.xilinx.com

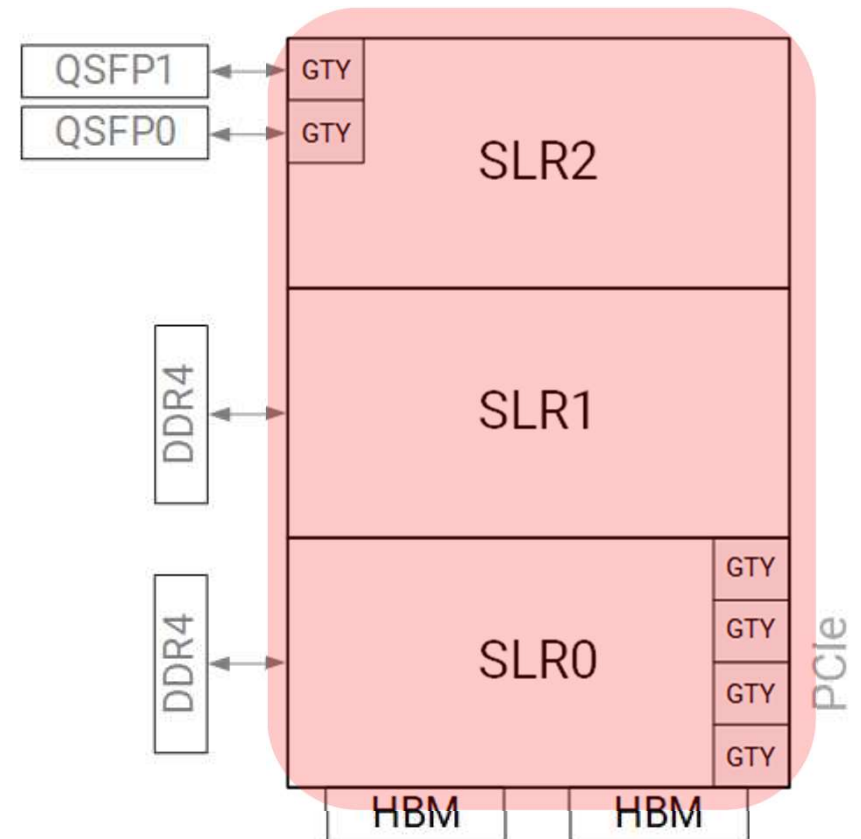
FPGAs: 10 inches view

- U200 FPGA connectivity & layout
 - DDR -> Global memory (RAM)
 - QSFP -> Ethernet 100Gb.
 - PCIe -> to host
 - USB -> serial line, jtag
- Super Logic Regions (SLR)
 - Logic partitions of the area of the FPGA
 - Connectors attached to SLRs



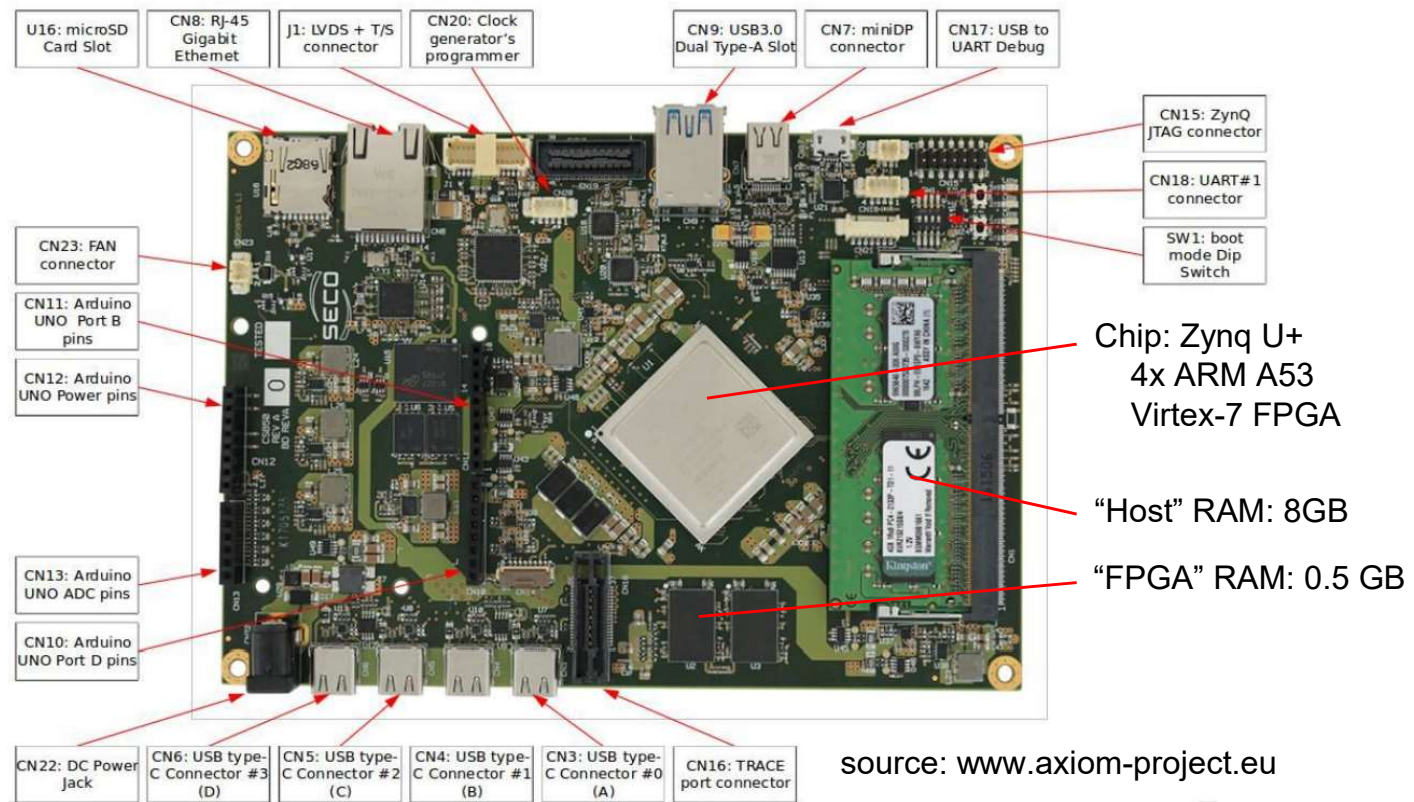
FPGAs: 10 inches view

- U280 FPGA connectivity & layout
 - DDR -> Global memory (RAM)
 - HBM -> Global memory (HBM)
 - QSFP -> Ethernet 100Gb.
 - PCIe -> to host
 - USB -> serial line, jtag



FPGAs: 10 inches view

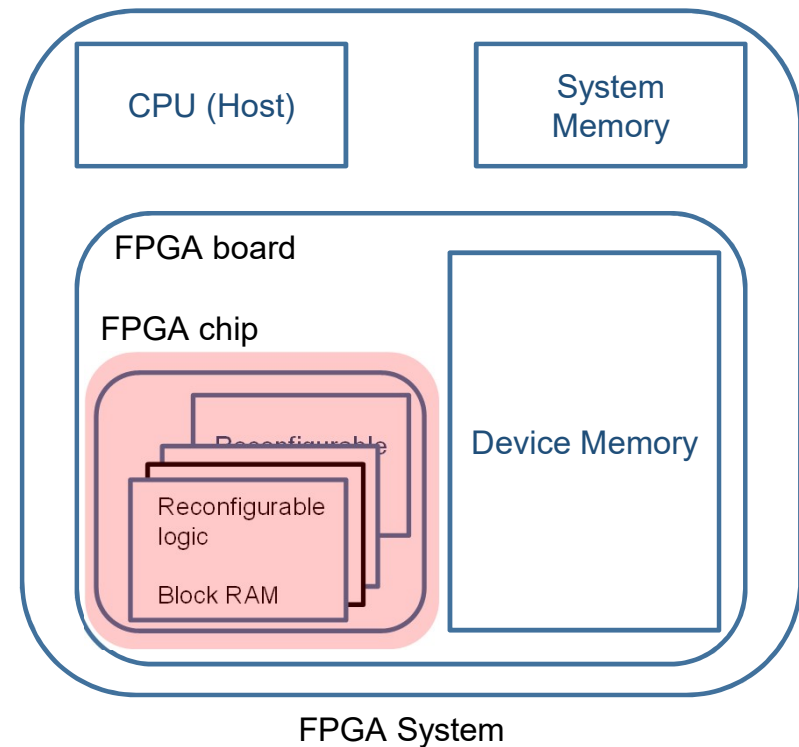
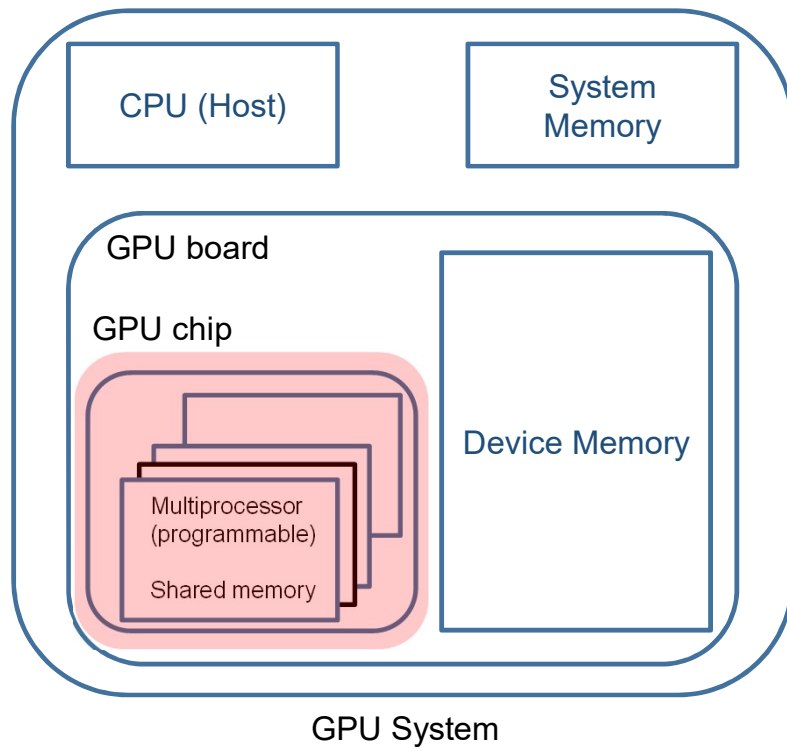
- Axiom board connectivity and layout



source: www.axiom-project.eu

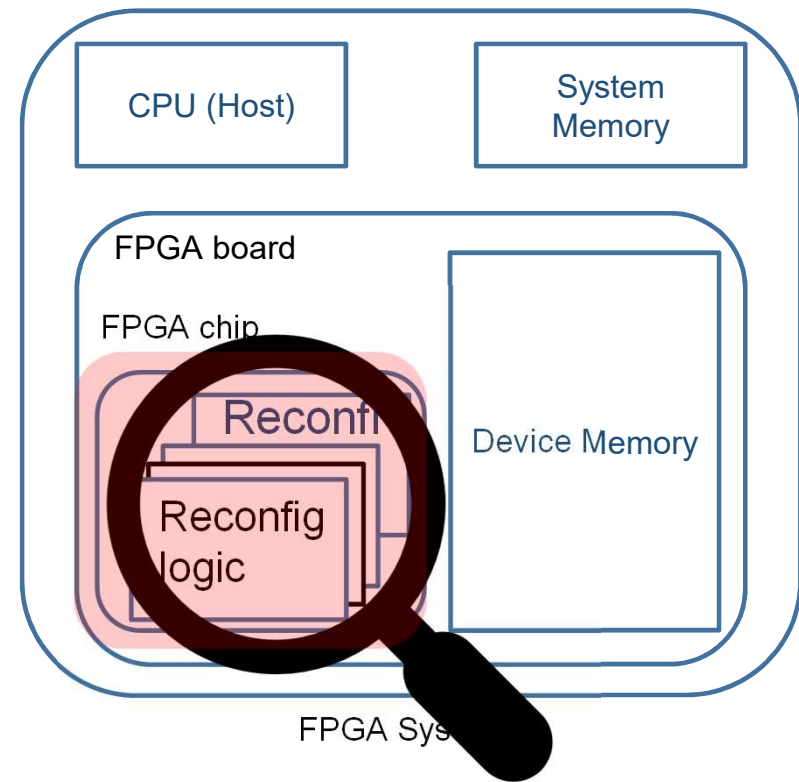
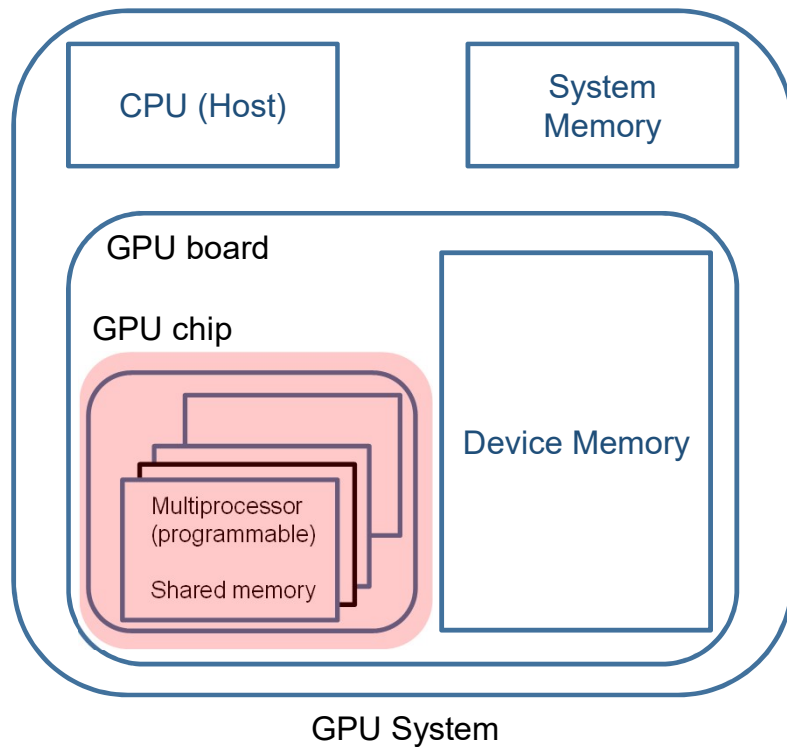
Comparing FPGAs to GPUs

- “Basically”, replace the GPU compute device with the FPGA device



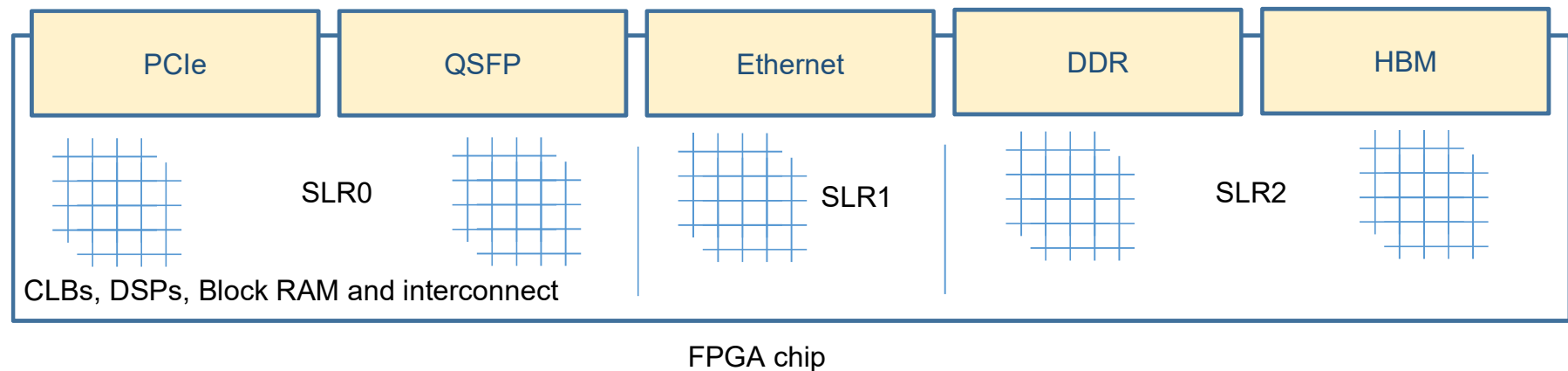
Comparing FPGAs to GPUs

- “Basically”, replace the GPU compute device with the FPGA device



Inside the FPGA chip

- Interfaces
- Super Logic Regions (SLRs)
 - Only on big devices (Alveo)
- Components: Configurable Logic Blocks (CLBs)

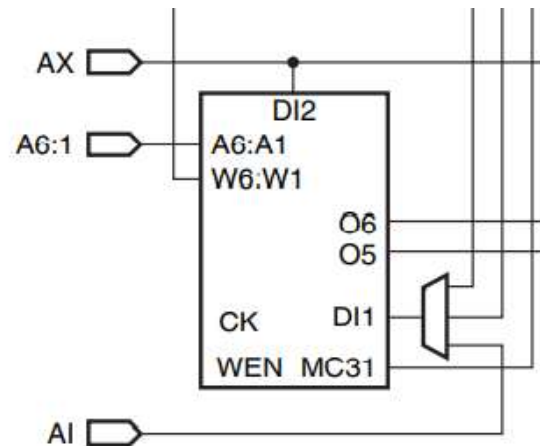


SLR components

- CLB (Configurable Logic Block)
 - Carry chain (adder, counter, comparator...)
 - Multiplexer (8 / 16 to 1)
 - Shift register
 - Flip-flop
 - Look-up tables (6-input)
 - Distributed RAM
 - Recommended for 1 to 128 bits data
- Block RAM
- DSP (Digital Signal Processing)

Sample components

- Look-up table (8 on a CLB)
 - 6 inputs (A6:1)
 - 2 outputs (O6:5)
 - 128 bits total



Available resources

ZU+: 274K

U200: 388K + 205K + 385K

U250: 420K + 205K + 407K + 424K

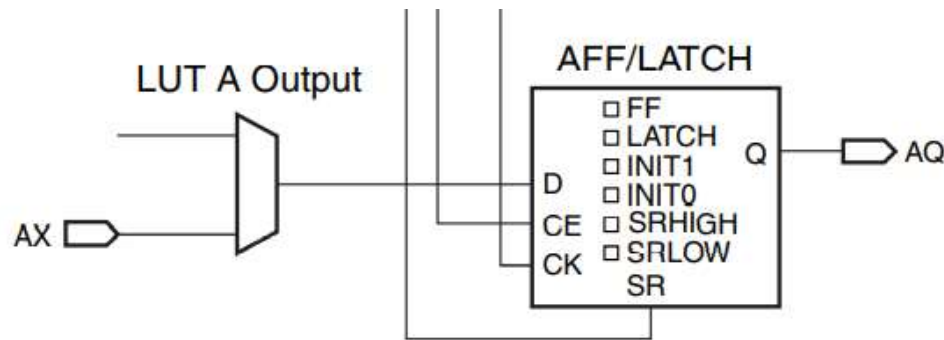
Sample components

- D flip-flop / latch (16 on a CLB)
 - 1 bit memory
 - Can take output from LUT A

Available resources
ZU+: 548K

U200: 776K + 410K + 770K

U250: 840K + 411K + 815K + 849K



Sample components

- Block RAM

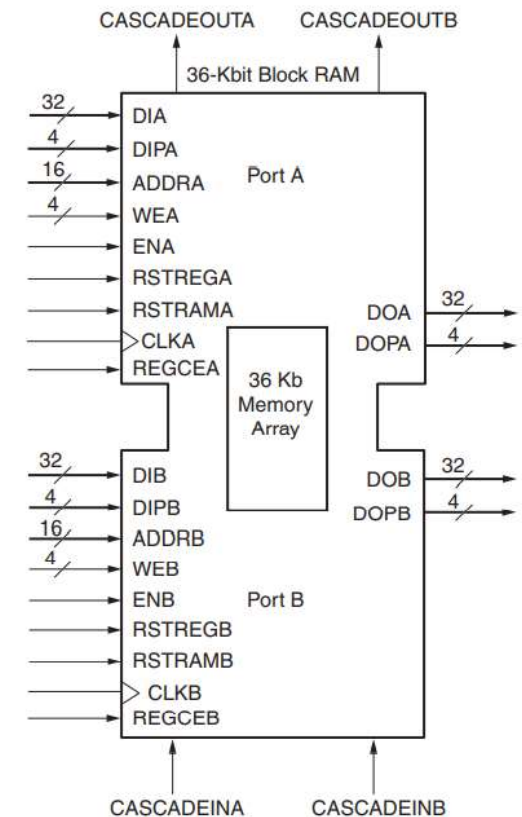
- Dual-port 36Kb
- Programmable FIFO
- Configurable width
 - 32Kb x 1 ... 4Kb x 8 ... 1Kb x 36

Available resources
ZU+: 32Mbit

U200: 25Mb + 13Mb + 25Mb
U250: 18Mb * 4

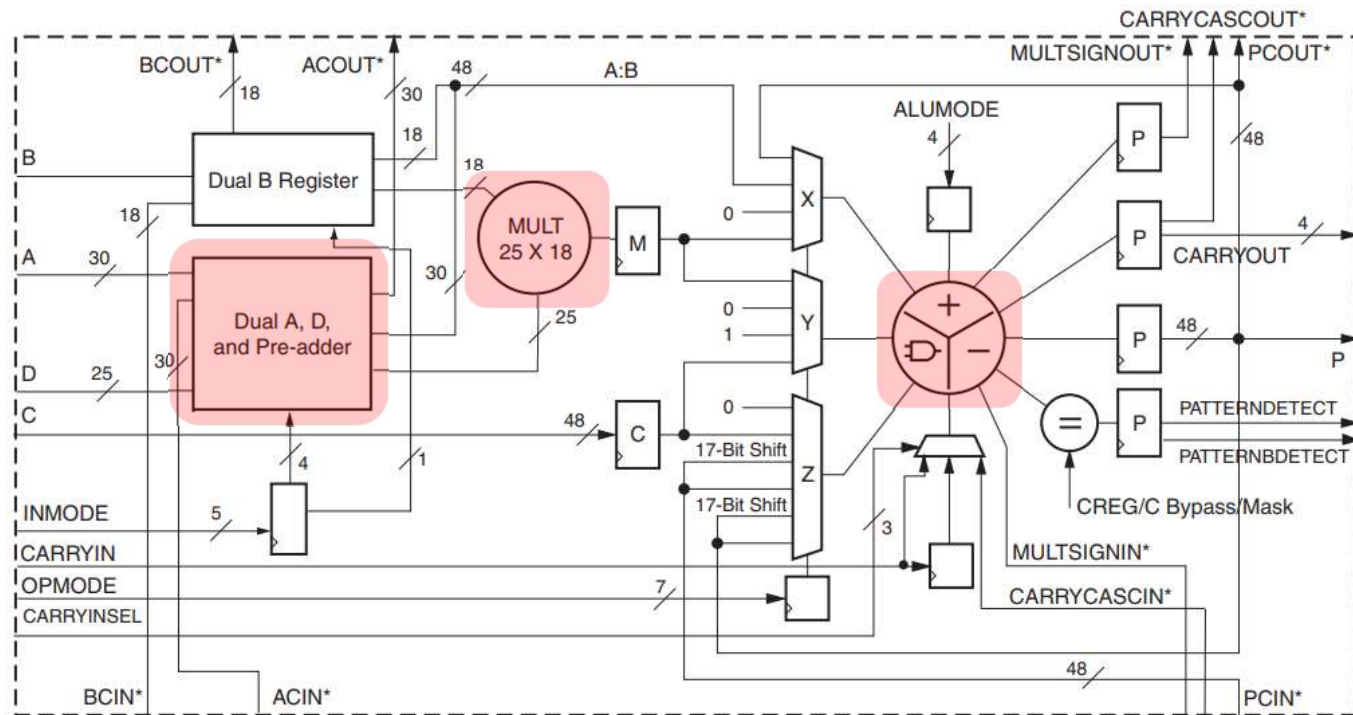
- Advise

- Use as many blocks as possible to achieve data parallelism



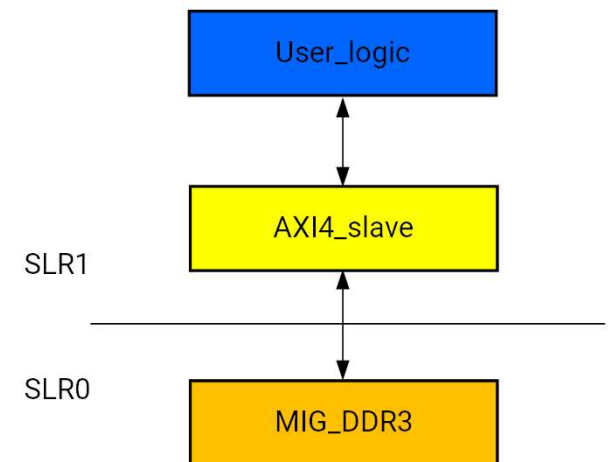
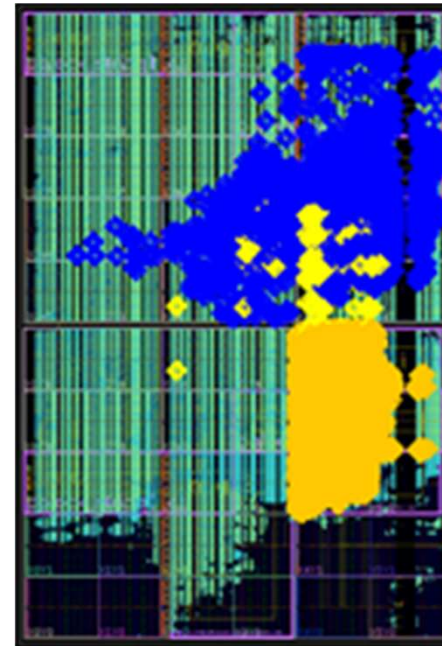
Sample components

- DSPs (48-bit)
 - Multiplier
 - Accumulator
 - Pre-adder
 - $C + B*(D+A) + \text{Carryin}$
 - SIMD unit (+, - only)
 - 2x24bit, 3x12bit
 - Logic unit
 - And, or, xor...
 - Pattern detector
 - Detect output pattern, or
 - C match with $A*B$...



Sample design

- Memory accesses are driven by the MIG (Memory Interface Generator)
- Interconnects are implemented with the AXI ports
- User logic contains the application



Generating FPGA configurations

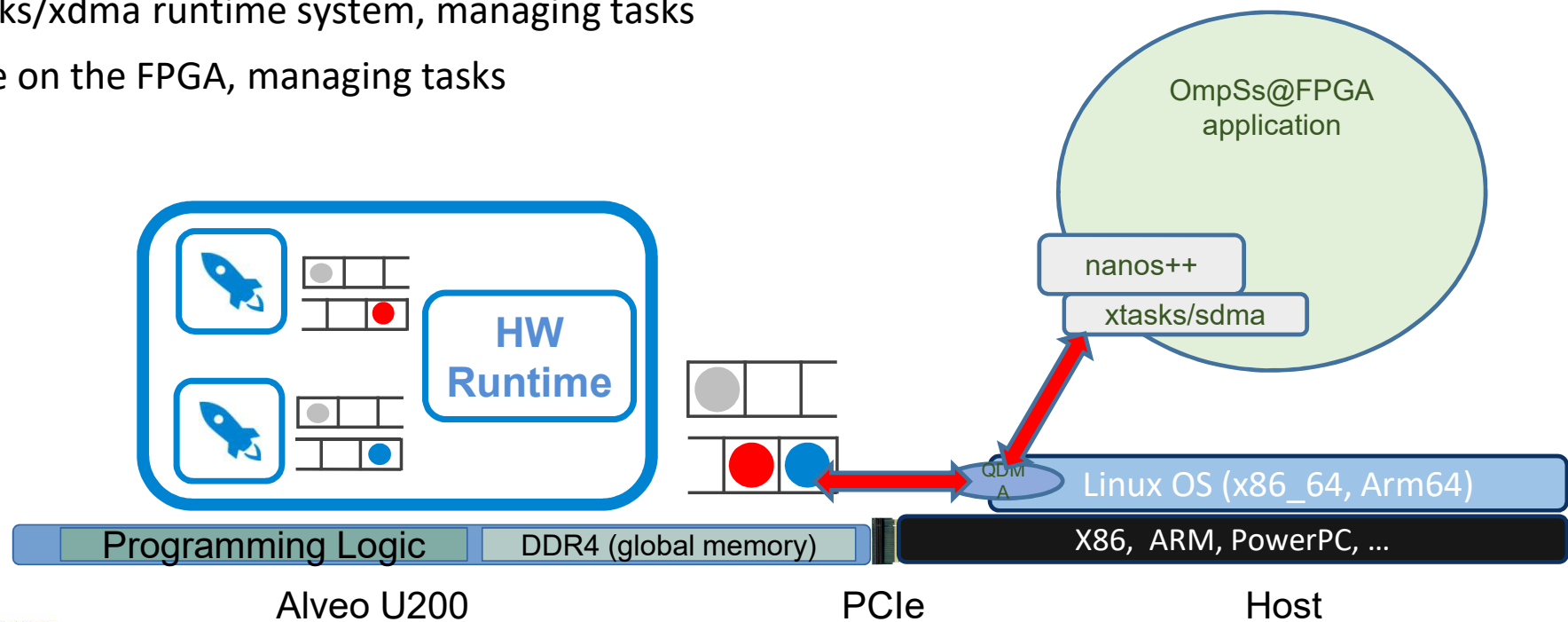
- High-level C/C++ programming
 - No Fortran support from vendors (as far as we know)
 - Compiled to Verilog/VHDL
- Design source files
 - Behavioral simulation
- Design synthesis, HDL to gates, generating FPGA netlists
 - Functional verification
- Design implementation, place & route
 - Static timing analysis
- Bitstream generation
 - Actual run on the FPGA

Vendor tools

- AMD - Xilinx
 - Vivado HLS / **Vitis HLS** (from 2020)
 - Vivado / **Vitis**
 - GUI and batch tools
 - Compile C/C++ code and OpenCL kernels
- Intel – Altera
 - Quartus HLS compiler
 - Quartus Prime Design Software
 - GUI and batch tools
 - Compile C/C++ code and OpenCL kernels
 - Also supports the **oneAPI** interface
 - Originated from Codeplay/Khronos SYCL
 - Kernels on C++ Lambda functions

OmpSs@FPGA execution environment

- x86_64 / Arm64 architectures
- Linux (Host), QDMA driver
- Nanos/xtasks/xdma runtime system, managing tasks
- Hw runtime on the FPGA, managing tasks



References

- References
 - DS962 – Alveo U200 and U250 Data Center Accelerator Cards Data Sheet
 - <https://docs.xilinx.com/r/en-US/ds962-u200-u250>
 - 7 Series FPGAs Configurable Logic Block. User Guide. Xilinx, Inc., UG474, 2016
 - https://docs.xilinx.com/v/u/en-US/ug474_7Series_CLB
 - 7 Series DSP48E1 Slice
 - https://docs.xilinx.com/v/u/en-US/ug479_7Series_DSP48E1
 - 7 Series FPGAs Memory Resources User Guide
 - https://docs.xilinx.com/v/u/en-US/ug473_7Series_Memory_Resources

References

- References
 - FPGA configuration generation steps
 - <https://hardwarebee.com/fpga-design/>

Introduction to FPGAs Hardware

Thank you!!